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(FILE 'HOME' ENTERED AT 09:55:41 ON 21 FEB 2003)

FILE 'EUROPATFULL, PCTFULL, USPATFULL, USPAT2' ENTERED AT 09:55:48 ON 21
FEB 2003

L1 1246166 S LOGIC OR PERIPHER?
L2 54920 S (IMPURIT? OR DOP?) (5A)CONCENTRAT?
L3 440727 S GATE#
L4 67766 S WORD#(2W)LINE# OR WORDLINE# OR WL#
L5 1360553 S CELL# OR MEMORY
L6 4344 S L2(7A)L3
L7 97 S L2(7A)L4
L8 18 S L6(P)L7
L9 308329 S L1(P)L5
L10 10 S L8 AND L9

=> d 4 6 7 bib ab

L10 ANSWER 4 OF 10 USPATFULL
AN 2003:30495 USPATFULL
TI Method of planarizing non-volatile memory device
IN Cho, Min-Soo, Seongnam-si, KOREA, REPUBLIC OF
Kim, Dong-Jun, Suwon-si, KOREA, REPUBLIC OF
Ryu, Eui-Youl, Yongin-si, KOREA, REPUBLIC OF
Kim, Dai-Goun, Incheon Gwangyeok-si, KOREA, REPUBLIC OF
Kim, Young-Hee, Yongin-si, KOREA, REPUBLIC OF
Hah, Sang-Rok, Seoul, KOREA, REPUBLIC OF
Kim, Kwang-Bok, Gapyeong-gun, KOREA, REPUBLIC OF
Nam, Jeong-Lim, Suwon-si, KOREA, REPUBLIC OF
Kim, Kyung-Hyun, Seoul, KOREA, REPUBLIC OF
PA Samsung Electronics Co., Ltd. (non-U.S. corporation)
PI US 2003022442 A1 20030130
AI US 2002-206511 A1 20020725 (10) *here we good*
PRAI KR 2001-45070 20010726
DT Utility
FS APPLICATION
LREP Steven M. Mills, MILLS & ONELLO LLP, Eleven Beacon Street, Suite 605,
Boston, MA, 02108
CLMN Number of Claims: 27
ECL Exemplary Claim: 1
DRWN 29 Drawing Page(s)
LN.CNT 785
AB Disclosed is a method of planarizing a non-volatile **memory**
device. After forming a floating gate structure on a **cell** area
of a semiconductor substrate, a conductive layer, a hard mask layer and
a first insulating layer are sequentially formed on the entire surface
of the resultant structure. After removing the first insulating layer
of
the **cell** area to leave a first insulating layer pattern only
on the **peripheral** circuit area, the hard mask layer of the
cell area is removed. A second insulating layer is formed on the
conductive layer and the insulating layer pattern to increase the
height
of the insulating layer on the **peripheral** circuit area. The
second insulating layer and the first insulating layer pattern are

removed until the floating gate structure is exposed, thereby planarizing the **cell** area and the **peripheral circuit** area. The conductive layer is patterned to form wordlines on both sidewalls of the floating gate structure and simultaneously, to form a gate of a **logic** device on the **peripheral circuit** area. When a CMP process for forming the wordline is carried out, the excessive polishing of the **cell** area adjacent to the **peripheral circuit** area can be prevented.

L10 ANSWER 6 OF 10 USPATFULL
AN 2002:20786 USPATFULL
TI Semiconductor device having both **memory** and **logic** circuit and its manufacture
IN Ohkawa, Narumi, Kawasaki-shi, JAPAN
PA FUJITSU LIMITED, Kawasaki, JAPAN (non-U.S. corporation)
PI US 2002011619 A1 20020131
AI US 2001-961264 A1 20010925 (9)
RLI Division of Ser. No. US 1999-288302, filed on 8 Apr 1999, PENDING
PRAI JP 1998-281699 19981002
DT Utility *application*
FS APPLICATION
LREP ARMSTRONG, WESTERMAN, HATTORI,, MCLELAND & NAUGHTON, LLP, 1725 K STREET, NW, SUITE 1000, WASHINGTON, DC, 20006
CLMN Number of Claims: 15
ECL Exemplary Claim: 1
DRWN 12 Drawing Page(s)
LN.CNT 1180
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A gate insulating film is formed on the principal surface of a semiconductor substrate. A silicon film is formed on the gate insulating film. Impurities are doped in the silicon film. In this case, impurities are doped into the silicon film to make a region of the silicon film in the **memory cell** area have a first impurity concentration and to make a region of the silicon film in the **logic** circuit area have a second impurity concentration lower than the first impurity concentration. The doped silicon film is patterned. In this case, the silicon film is patterned to leave word lines having the first **impurity concentration** and serving as **gate** electrodes in the **memory cell** area and to leave **gate** electrodes having the second **impurity concentration** in the **logic** circuit area. Source/drain regions of MISFET's are formed in a surface layer of the semiconductor substrate by doping impurities into regions on both sides of each word line in the **memory cell** area and into regions on both sides of each gate electrode in the **logic** circuit. The electrical characteristics of the **logic** circuit area can be improved while the data storage characteristics of **memory cells** are maintained good.

L10 ANSWER 7 OF 10 USPATFULL
AN 2001:221321 USPATFULL
TI Semiconductor device having both **memory** and **logic** circuit and its manufacture
IN Ohkawa, Narumi, Kawasaki, Japan
PA Fujitsu Limited, Kawasaki, Japan (non-U.S. corporation)
PI US 6326657 B1 20011204
AI US 1999-288302 19990408 (9) *Patent*
PRAI JP 1998-281699 19980210
DT Utility
FS GRANTED
EXNAM Primary Examiner: Lee, Eddie; Assistant Examiner: Ortiz, Edgardo
LREP Armstrong, Westerman, Hattori, McLeland & Naughton, LLP

CLMN Number of Claims: 8

ECL Exemplary Claim 1

DRWN 27 Drawing Figure(s); 12 Drawing Page(s)

LN.CNT 1058

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AB A gate insulating film is formed on the principal surface of a semiconductor substrate. A silicon film is formed on the gate insulating

film. Impurities are doped in the silicon film. In this case, impurities

are doped into the silicon film to make a region of the silicon film in the **memory cell** area have a first impurity concentration and to make a region of the silicon film in the

logic circuit area have a second impurity concentration lower than the first impurity concentration. The doped silicon film is patterned. In this case, the silicon film is patterned to leave **word lines** having the first **impurity concentration** and serving as **gate** electrodes in the

memory cell area and to leave **gate**

electrodes having the second **impurity concentration**

in the **logic** circuit area Source/drain regions of MISFET's are formed in a surface layer of the semiconductor substrate by doping impurities into regions on both sides of each word line in the **memory cell** area and into regions on both sides of each gate electrode in the **logic** circuit. The electrical characteristics of the **logic** circuit area can be improved while the data storage characteristics of **memory cells** are maintained good.

=> s 18 not 110

L11 8 L8 NOT L10

=> d 1-8 kwic

L11 ANSWER 1 OF 8 EUROPATFULL COPYRIGHT 2003 WILA

DET DEN Note that although the diffusion layer 37a should be a P-type and have a higher **concentration** than the **impurity concentration** of the channel directly below the **word** line 38, the diffusion layer may not be formed. Further, in the case where the diffusion layer 37a is formed at. . . The . . . the case where the thickness of the second element separation oxide film 43 is the same as that of the **gate** oxide film 42, the **impurity concentration** of the P-type regions 44a and 44c should be higher than that of the channel formed underneath the gate electrodes. . .

L11 ANSWER 2 OF 8 EUROPATFULL COPYRIGHT 2003 WILA

DET DEN Figure 1 is a cross-sectional view of a MIS transistor;

Fig. 2 is a graph of an **impurity concentration** in a poly Si **gate**, a SiO₂ gate insulating film, and a Si substrate;

Fig. 3 shows a cross-sectional view of a stacked type. . . Figure 1 is a cross-sectional view of a MIS transistor;

Fig. 2 is a graph of an **impurity concentration** in a poly Si **gate**, a SiO₂ gate insulating film, and a Si substrate;

Fig. 3 shows a cross-sectional view of a stacked type. . . The relationship between the **gate** insulating film thickness and the **impurity concentration** in the MIS transistor will be explained with reference to Figures 1 and 2. The relationship between the **gate** insulating film thickness and the **impurity concentration** in the MIS

transistor will be explained with reference to Figures 1 and 2. Figure 2 shows a graph of an **impurity concentration** in a poly Si **gate** (C.sub1.), a SiO₂ gate insulating film (C.sub2.), and a Si substrate (C.sub3.), wherein the transverse axis shows the depth, and. . .

Figure 2 shows a graph of an **impurity concentration** in a poly Si **gate** (C.sub1.), a SiO₂ gate insulating film (C.sub2.), and a Si substrate (C.sub3.), wherein the transverse axis shows the depth, and. . .

Then, . . . a usual photolithography technique, so that a MIS semiconductor device providing poly Si electrode interconnection or wiring 17 having low **impurity concentration**

n.supmin. **gate** electrode portions 17A.sub1. and 17A.sub2.

with a high sheet resistance and a high impurity concentration n.supplus. interconnection or wiring portions. . .

Then, . . . a usual photolithography technique, so that a MIS semiconductor device providing poly Si electrode interconnection or wiring 17 having low **impurity concentration**

n.supmin. **gate** electrode portions 17A.sub1. and 17A.sub2.

with a high sheet resistance and high impurity concentration n.supplus. interconnection or wiring portions 17B.sub1.. . .

In a **gate** electrode WL1, **impurities** for example, phosphorus having a **concentration** of 10.sup2..sup0. to 10.sup2..sup1./cm.sup3. are introduced thereto. The thickness of

the

insulating layer below the gate electrode WL1 is about. . .

In a **gate** electrode WL1, **impurities** for example, phosphorus having a **concentration** of 10.sup2..sup0. to 10.sup2..sup1./cm.sup3. are introduced thereto. The thickness of

the

insulating layer below the gate electrode WL1 is about. . .

L11 ANSWER 3 OF 8 USPATFULL

SUMM As illustrated in FIG. 1, a conventional mask ROM has a buried oxide layer 19 which is perpendicular to a **wordline of gate** 23. A high **concentration impurity** region (not shown) made of a common source and drain region and used for a bit line is formed under. . .

L11 ANSWER 4 OF 8 USPATFULL

SUMM As illustrated in FIG. 1, a conventional mask ROM has a buried oxide layer 19 which is perpendicular to a **wordline of gate** 23. A high **concentration impurity** region (not shown) made of a common source and drain region and used for a bit line is formed under. . .

L11 ANSWER 5 OF 8 USPATFULL

DETD . . . poly 54 of the inventive cell is in contrast with a conventionally formed E.sup.2 PROM cell which has a heavily **doped floating gate poly**. The **concentration** of the **dopant** (for example phosphorous, arsenic, or antimony) in the lightly doped regions can be from about 10.sup.16 -10.sup.18 atoms/cm.sup.3 or to other workable **concentrations**. Next, the **doped word line** 14 is formed over the floating gate poly 52. An angled implant heavily dopes one edge of the floating gate. . .

L11 ANSWER 6 OF 8 USPATFULL

DETD . . . poly 54 of the inventive cell is in contrast with a conventionally formed E.sup.2 PROM cell which has a heavily **doped floating gate poly**. The **concentration** of the **dopant** (for example phosphorous, arsenic, or antimony) in the lightly doped regions can be from about 10.sup.16 -10.sup.18 atoms/cm.sup.3 or to other workable **concentrations**. Next, the **doped word line** 14 is formed over the

floating gate ly 52. An angled implant heavily dopes one edge of the floating gate . . .

L11 ANSWER 7 OF 8 USPATFULL

DETD In a **gate** electrode **WL1**, **impurities** for example, phosphorus having a **concentration** of to 10.sup.20 to 10.sup.21 /cm.sup.3 are introduced thereto. The thickness of the insulating layer below the gate electrode **WL1**. . .

L11 ANSWER 8 OF 8 USPATFULL

SUMM . . . the ratio V.sub.G2S(OFF) /V.sub.G1S(OFF) of pinch-off voltages between the gate and source is directly caused by variation in the ratio

W2/W1 of the channel widths and **impurity concentration** of the diffusion layers of junction **gates** 15 and 16. Further, it is affected by the impurity concentration and diffusion depth of the diffusion layer formed in. . .

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L4 67766 S WORD# (2W) LINE# OR WORDLINE# OR WL#
L5 1360553 S CELL# OR MEMORY
L6 4344 S L2(7A)L3
L7 97 S L2(7A)L4
L8 18 S L6(P)L7
L9 308329 S L1(P)L5
L10 10 S L8 AND L9
L11 8 S L8 NOT L10

=> d 2 bib ab

L11 ANSWER 2 OF 8 EUROPATFULL COPYRIGHT 2003 WILA

PATENT APPLICATION - PATENTANMELDUNG - DEMANDE DE BREVET

AN 329569 EUROPATFULL ED 20000924 EW 198934 FS OS STA B
TIEN Semiconductor device with a thin insulating film.
TIDE Halbleiteranordnung mit einer duennen isolierenden Schicht.
TIFR Dispositif semi-conducteur ayant une mince couche isolante.
IN Ema, Taiji, Enzeru haimu Shinjo 101 1453-1, Suenaga Takatsu-ku,
Kawasaki-shi Kanagawa 213, JP;
Shirai, Kazunari, Paaku saido Hodogaya 313 1310-4, Bukkou-cho,
Hodogaya-ku Yokohama-shi Kanagawa 240, JP
PA FUJITSU LIMITED, 1015, Kamikodanaka Nakahara-ku, Kawasaki-shi Kanagawa
211, JP
PAN 211460
AG Joly, Jean-Jacques et al, CABINET BEAU DE LOMENIE 55, rue d'Amsterdam,
F-75008 Paris, FR
AGN 39741
OS ESP1989035 EP 0329569 A2 890823
SO Wila-EPZ-1989-H34-T2
DT Patent
LA Anmeldung in Englisch; Veröffentlichung in Englisch
DS R DE; R FR; R GB
PIT EPA2 EUROPAEISCHE PATENTANMELDUNG

PI	EP 329569	A2 19890823
OD		19890823
AI	EP 1989-400463	19890217
PRAI	JP 1988-34346	19880217

GRANTED PATENT - ERTEILTES PATENT - BREVET DELIVRE

AN 329569 EUROPATFULL UP 20010720 EW 199527 FS PS STA B
TIEN Semiconductor device with a thin insulating film.
TIDE Halbleiteranordnung mit einer duennen isolierenden Schicht.
TIFR Dispositif semi-conducteur ayant une mince couche isolante.
IN Ema, Taiji, Enzeru haimu Shinjo 101 1453-1, Suenaga Takatsu-ku,
Kawasaki-shi Kanagawa 213, JP;
Shirai, Kazunari, Paaku saido Hodogaya 313 1310-4, Bukkou-cho,
Hodogaya-ku Yokohama-shi Kanagawa 240, JP
PA FUJITSU LIMITED, 1015, Kamikodanaka Nakahara-ku, Kawasaki-shi Kanagawa
211, JP
PAN 211460
AG Joly, Jean-Jacques et al, Cabinet Beau de Lomenie 158, rue de
l'Universite, F-75340 Paris Cedex 07, FR
AGN 39741
OS EPB1995050 EP 0329569 B1 950705
SO Wila-EPS-1995-H27-T2
DT Patent
LA Anmeldung in Englisch; Veroeffentlichung in Englisch
DS R DE; R FR; R GB
PIT EPB1 EUROPAEISCHE PATENTSCHRIFT
PI EP 329569 B1 19950705
OD 19890823
AI EP 1989-400463 19890217
PRAI JP 1988-34346 19880217
REP EP 12863 A FR 2133893 A
US 3897282 A
ABEN A semiconductor device comprises :
a insulating film (26, 25) having first part (26) and a second
part (25), the second part (25) being thinner than the first part (26); and
a polycrystalline silicon film having a first part (23) arranged over
the first part (26) of the insulating film and a second part (24)
arranged over the second part (25) of the insulating film, the second
part (24) of the polycrystalline silicon film having a lower
concentration of impurities than that of the first part of
polycrystalline silicon film.

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L8 18 S L6 (P) L7
L9 308329 S L1 (P) L5
L10 10 S L8 AND L9
L11 8 S L8 NOT L10
L12 2680 S L1 (P) L2 (P) L3
L13 1142 S L2 (P) L4 (P) L5
L14 365 S L12 (P) L13
L15 498 S L6 (P) L1
L16 52 S L7 (P) L5
L17 6 S L15 AND L16

=> file japiro

COST IN U.S. DOLLARS	SINCE FILE ENTRY	TOTAL SESSION
FULL ESTIMATED COST	79.77	79.98

FILE 'JAPIO' ENTERED AT 10:31:25 ON 21 FEB 2003
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FILE LAST UPDATED: 10 FEB 2003 <20030210/UP>
FILE COVERS APR 1973 TO OCTOBER 31, 2002

<<< GRAPHIC IMAGES AVAILABLE >>>

=> s 18

82288 IMPURIT?
30902 DOP?
140772 CONCENTRAT?
170500 GATE#
82288 IMPURIT?
30902 DOP?
140772 CONCENTRAT?
57418 WORD#
561093 LINE#
15 WORDLINE#
2960 WL#
L18 1 L6 (P) L7

=> d ab

L18 ANSWER 1 OF 1 JAPIO COPYRIGHT 2003 JPO
AB PROBLEM TO BE SOLVED: To obtain a method of manufacturing a semiconductor

device which enables the electric characteristics of a logic circuit part to be enhanced while favorably keeping the data-hold characteristics of a memory cell.

SOLUTION: A gate insulation film is formed on the main surface of a semiconductor substrate. A silicon film is formed on the gate insulation film. An impurity is added to the silicon film. The impurity is added to the area over a memory cell part of the silicon film so as to have a first

impurity concentration, and to the area over a logic circuit part so as to

have a second impurity concentration which is lower than the first **impurity concentration**. The silicon film is patterned. A

word line 8a which also serves as a **gate**

electrode 8b and has the first **impurity concentration**

is left at the memory cell part, and the **gate** electrode 8b which has the second **impurity concentration** is left at the

logic circuit part. An impurity is added to the area at both sides of the word line of the memory cell part and the area at both sides of the gate electrode 8b of the logic circuit part of the surface layer of the semiconductor substrate to form the source/drain area 9a of a MISFET.

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L18 ANSWER 1 OF 1 JAPIO COPYRIGHT 2003 JPO

AN 2000-114471 JAPIO

TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

IN OKAWA SHIGEMI

PA FUJITSU LTD

PI JP 2000114471 A 20000421 Heisei

AI JP 1998-281699 (JP10281699 Heisei) 19981002

PRAI JP 1998-281699 19981002

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000

AB PROBLEM TO BE SOLVED: To obtain a method of manufacturing a semiconductor device which enables the electric characteristics of a logic circuit part to be enhanced while favorably keeping the data-hold characteristics of a memory cell.

SOLUTION: A gate insulation film is formed on the main surface of a semiconductor substrate. A silicon film is formed on the gate insulation film. An impurity is added to the silicon film. The impurity is added to the area over a memory cell part of the silicon film so as to have a first

impurity concentration, and to the area over a logic circuit part so as to

have a second impurity concentration which is lower than the first **impurity concentration**. The silicon film is patterned. A

word line 8a which also serves as a **gate**

electrode 8b and has the first **impurity concentration**

is left at the memory cell part, and the **gate** electrode 8b which has the second **impurity concentration** is left at the

logic circuit part. An impurity is added to the area at both sides of the word line of the memory cell part and the area at both sides of the gate electrode 8b of the logic circuit part of the surface layer of the semiconductor substrate to form the source/drain area 9a of a MISFET.

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